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A Low Power Design Approach for the Implementation of Ternary Logic

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Abstract

This paper presents the design and simulation of a ternary CMOS SRAM cell. Ternary Logic is a promising alternative to the conventional binary logic as it reduces the number of interconnects which occupy a large area on a VLSI chip and thereby helps in accomplishing simplicity and energy efficiency. The ternary SRAM was created using cross-coupled ternary inverters using PSPICE 9.1. The inverters were optimized for high noise margins and the optimum transistor sizings were presented.

Keywords

Simple Ternary Inverter (STI); Negative Ternary Inverter(NTI); Positive Ternary Inverter(PTI).

Introduction

There is a tremendous rise in the demand for low power devices and the devices with small chip area. Mostly all electronics used today is based on binary logic and in a VLSI circuits, approximately 70 percent of the area is devoted to interconnection, 20 percent to insulation, and 10 percent to devices. The binary logic is limited due to interconnect which occupies large area on a VLSI chip. One can achieve a more cost effective way of utilizing interconnections by using a larger set of signals over the same area in multiple-valued logic (MVL) circuits. Therefore the higher radix logic, mainly known as Multi Valued logic (MVL) has been implemented in the past and has attracted considerable interests due to its potential advantages over binary logic for designing of digital systems. As the optimal base for developing hardware is proven to be 2.71, the closest integer to this optimal base is base 3, which corresponds to the ternary numbering system.

The CMOS logic implemented currently is mostly based on radix-2 or binary logic. The higher radix logic is mainly known as Multi Valued logic (MVL). It has been implemented

in the past and has attracted considerable interests due to its potential advantages over binary logic for designing of digital systems but out of so many multi valued logics only ternary logic has been chosen because (a) Since 3 is the smallest radix higher than binary, ternary functions and circuits have the simpler form and construction, (b) As a measure of the cost or complexity of multivalued circuits, the product of the radix and the number of signals has been proposed. Since 3 is the digit nearest to e = 2.718, ternary circuits will be more economical according to this measure, (c) If balanced ternary logic (1, 0, - 1) is used, the same hardware may be used for addition and for subtraction, (d) Since 3 is not an integral power of 2, research on ternary logic may disclose design techniques that are overlooked in the study of binary or quaternary logic.

There are several advantages of using ternary logic as by using ternary logic each wire can transmit more MVL information than binary hence the number of connections inside the chip can be reduced which indeed reduces the chip area and power dissipation. Besides these advantages ternary logic also has some disadvantages because as the logic level increases the tolerance of the circuit becomes more critical and due to multi valued signals the complexity of the circuit also increases.

Ternary Logic and Building Blocks

Ternary logic functions are those functions that have significance if a third value is introduced to the binary logic. In this paper, 0, 1, and 2 denote the ternary values to represent false, undefined, and true, respectively. The three types of inverters that are presented in this paper are Simple Ternary Inverter, Positive Ternary Inverter and Negative Ternary Inverter.

A. Simple Ternary Inverter(STI)

The first type of ternary inverter is the simple ternary inverter (STI). For the inputs {0, 1, 2} it yields the output {2, 1, 0}. Because of its ability to produce {1} at the output, STI is used as the primary building block for the proposed SRAM cell. A high resistance transmission gate is connected between the output of a low-resistance threshold modified binary inverter and 0.5Vs to produce the middle level voltage.

The Simple Ternary Inverter is made by combining a binary CMOS inverter with a transmission gate. The threshold voltages of the transistors in CMOS inverter were made half of the supply voltage while transistors of transmission gate were simulated with threshold voltages specified by the TSMC 180nm design parameters. The inverter works as a simple inverter when the input is 0V or 2V. But when the input is 1V, the transistors Q1 and Q2 goes in cut off region and the transmission gate aids in pulling up the control signal

(whose value is equal to the half of supply voltage), to the output when the inverter is in cut off region.

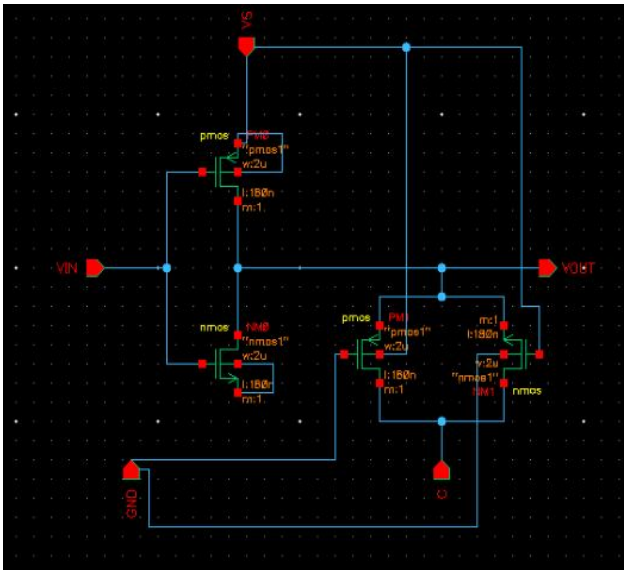

Fig.1. A circuit representation of Simple Ternary Inverter

B. Negative Ternary Inverter (NTI)

The Negative Ternary Inverter (NTI) was implemented using the same logic designs and sizing requirements. For the input of {0, 1, 2}, NTI provides the output {0, 0, 2}. An always on transistor (NMOS for NTI) is used for the passing the middle voltage instead of a transmission gate as its gate is tied to the positive power supply to keep it constantly ON.

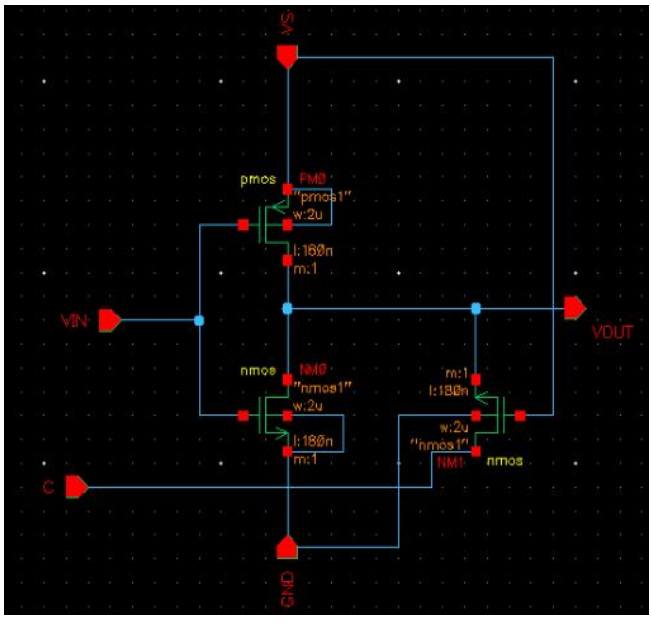

Fig.2. A circuit representation of Negative Ternary Inverter

It behaves as a normal inverter when the input voltage i.e. Vin is equal to 0V and 2V, but when the value of Vin is equal to 1V, the transistors Q1 and Q2 goes in cut off region and

the transmission gate aids in pulling up the control signal C (whose value is equal to 0Volts), to the output when the inverter is in cut off region. Therefore when the value of Vin is 1Volt the output of NTI is 0Volt.

C. Positive Ternary Inverter (PTI)

The Positive Ternary Inverter was implemented using the logic design and sizing requirements. An input of {0, 1, 2} provides {2, 2, 0} for output of PTI. In PTI, an additional always on transistor (PMOS for PTI) is used to pass middle voltage.

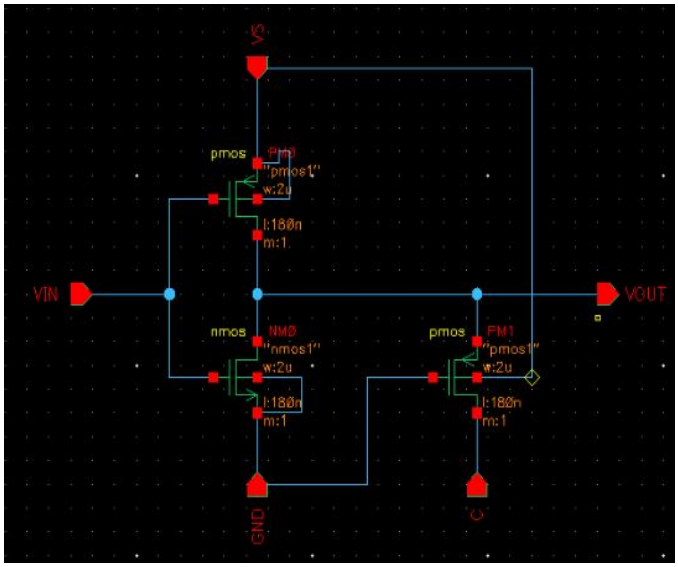

Fig.3. A circuit representation of Positive Ternary Inverter

PMOS transistor is connected to the output of CMOS inverter and its gate is tied to the ground, to keep it constantly turned ON. It behaves as a normal inverter when the input voltage i.e. Vin is equal to 0V and 2V, but when the value of Vin is equal to 1V, the transistors Q1 and Q2 goes in cut off region and the transmission gate aids in pulling up the control signal C (whose value is equal to 2Volts), to the output when the inverter is in cut off region. Therefore when the value of Vin is 1Volt the output of PTI is 2Volts.

Static Random Access Memory (SRAM)

Static Random Access Memory holds the data in static form, that is, as long as the power is supplied to it. A ternary SRAM is constructed by cross-coupling two STIs for the data storage element and adding two access transistors gated by a word line WORD between the stored data and bit lines (TRIT LINES).

The access transistors are used to access the stored data for read and write operation. The WORD Line, WL, is used to control the access. When WL = 0, hold operation is performed, and when WL = 1, read or write operation is performed by the SRAM.

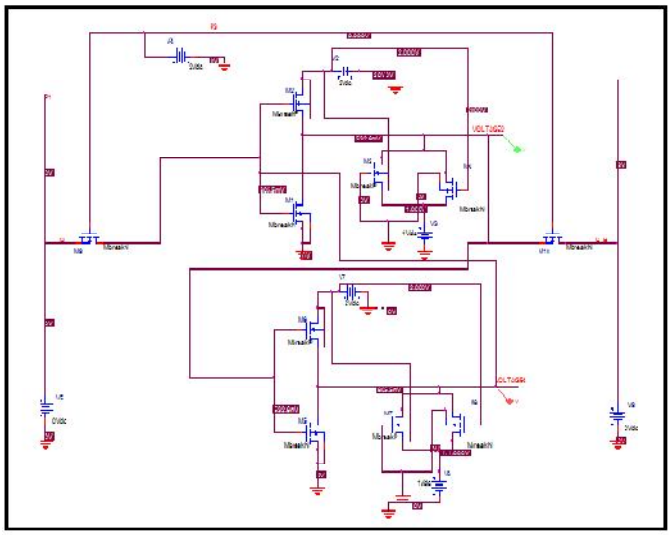

Fig. 4. A circuit representation of SRAM

The STI used in SRAM consist of four transistors each to make it a ternary SRAM. Ternary SRAM means that it will be capable of storing three values instead of two as in case of binary SRAM. The three values can be 0,1,2 or it can be -1,0,1 depending upon the logic circuitry used for making SRAM.

Simulation Results of SRAM

Cadence Virtuoso and PSPICE 9.1 were used in this paper for the implementation of Simple, Positive and Negative Inverter and SRAM. The advantage of using Ternary SRAM over binary SRAM is that the ternary SRAM is capable of storing three types of values, 0,1,2, whereas binary SRAM can store only two, that is, 0 or 1.

SRAM cell has three different states of operation. It can be in: standby (the circuit is idle), reading (the data has been requested) and writing (updating the contents). The SRAM to operate in read mode and write mode should have "readability" and "write stability" respectively. The three different states work as follows:

Writing- To write to the cell, TRIT Lines must be driven to the desired value while WORD is asserted to force the stored data to the value of TRIT. The value which is to be stored in SRAM must be given to the TRIT Lines and WORD Line must be asserted in order to keep access transistors ON.

In this case the value of TRIT Line passes through the access transistors to the first STI Inverter. If TRIT = 2, then the NMOS of first STI turns ON, which in turn makes the output of first STI low. As the output of first STI is connected to the input of second STI, it turns ON the PMOS of second STI which makes the output of second STI high. As the output of second STI is connected to the input of first STI, it again makes the output of first STI low and this is how the process goes on and both the STI support each other.
If the value that is to be written in the SRAM is 0 or 1 then voltage applied to the TRIT Lines must be 0 and 1 respectively.

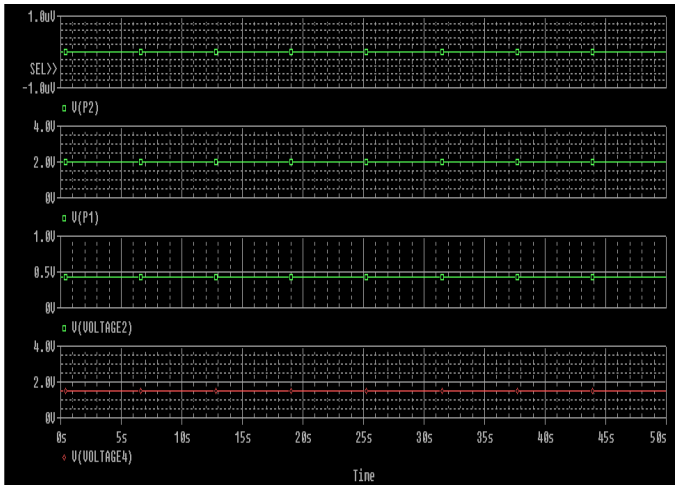

Fig.5. WRITE Operation in SRAM when Vp1=2V, Vp2=0V (TRIT Lines) and Vp3=2V (Word Line) (Stored value=2)

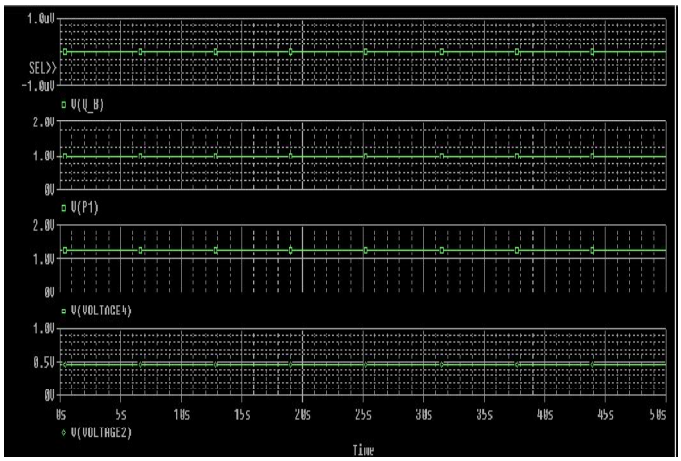

Fig.6. WRITE Operation in SRAM when Vp1=1V, Vp2=0V (TRIT Lines) and Vp3=2V(Word Line) (Stored value=1)

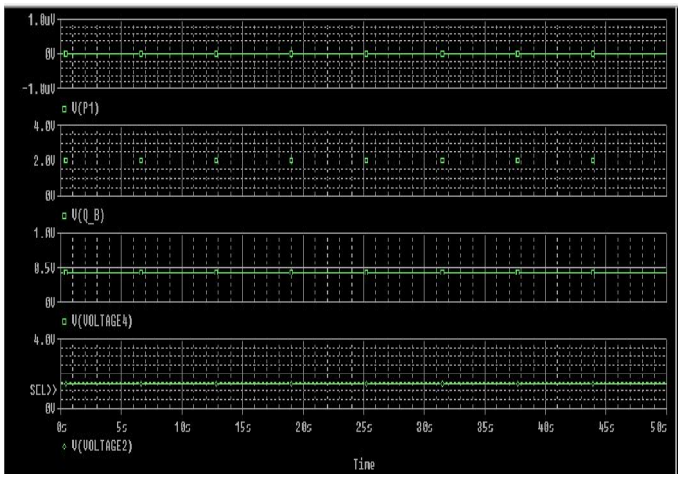

Fig.7. WRITE Operation in SRAM when Vp1=0V, Vp2=2V (TRIT Line) and Vp3=2V (Word Line) (Stored value=0)

Standby - If the word line is not asserted, i.e. WL=0, the access transistors disconnect the cell from the bit lines and the two cross-coupled inverters will continue to reinforce each other as long as they are connected to the supply.

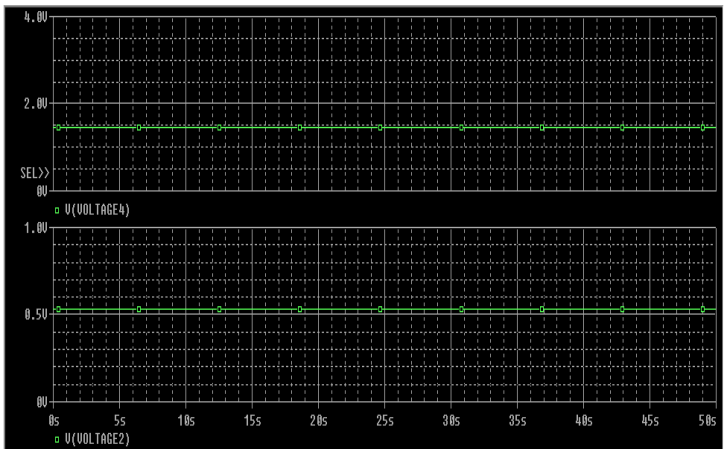

Fig.8. Standby Mode of SRAM when VP3=0V (Word Line)

Reading- To read the cell, TRIT must be left floating while WORD is asserted to force TRIT to the value of the stored data in Q. In this case, the capacitors are used in the TRIT Lines, which are precharged to half the value of the power supply by the use of PMOS transistors. The WORD Line is then asserted to turn ON the access transistors so that the stored value in the STI can go to the TRIT Line and the value can be read.

The value of the TRIT Lines is actually read by the sense by a simple differential amplifier. It compares the difference between the TRIT and TRIT_b Line. If TRIT > TRIT_b, then the output is 1 and if TRIT < TRIT_b, then the output is 0. It allows output to be set quickly without fully charging/discharging the TRIT line.

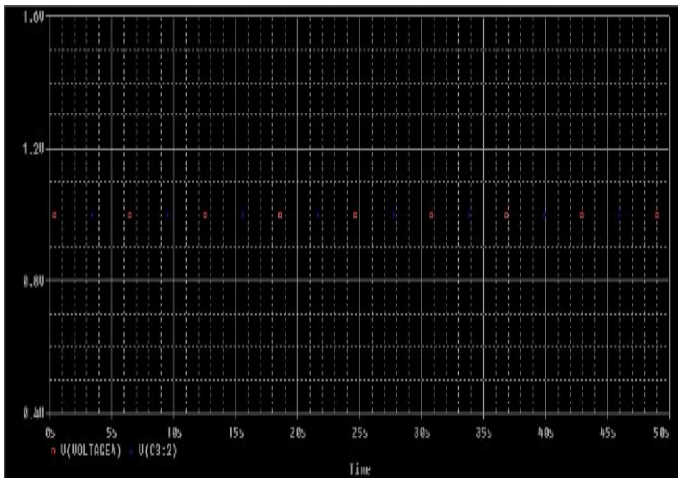

Fig.9. Reading Operation of SRAM when Vp1 and Vp2 were left floating and Vp3=2V

Conclusion

A technique for implementing the ternary logic circuits was successfully simulated and desired results were attained. It was seen that the implemented ternary SRAM is capable of storing three types of values, which are 0,1,2, and this is a advantage over binary SRAM as this reduces the number of interconnects to pass the same amount of information. As the number of interconnects reduces the chip area also reduces and hence the overall cost of the device is also reduced.

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